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MULTI-PORT MEMORY ARCHITECTURE

Abstract

A multi-port memory architecture utilizing an open bitline configuration for the read bitline is described. The memory is subdivided into two arrays (A and B) consisting of memory gain cells arranged in a matrix formation, the cells having two general ports or separate read and write ports to enable simultaneous a read and write operation. Each memory array includes a reference wordline coupled to reference cells. When the reference cell is accessed, the read bitline (RBL) discharges to a level at half the value taken by a cell storing a 0 or 1. Each pair of RBLB in the same column of the two arrays is coupled to a differential sense amplifier, and each write bitline (WBL) in the two arrays is linked to write drivers WBLs in the two arrays are driven to the same voltage and at the same slew rate. The WBL swing in each array creates coupling noise by the bitline-to-bitline capacitors. For a given sense amplifier and its associated RBLs, the coupling creates an identical coupling noise on RBLA and RBLB that are positioned in the two arrays A and B. This common mode noise is rejected by the differential sense amplifier. Thus, a read sense amplifier can accurately

discriminate between the signal by activating the cell by way of RWL, and the reference cell by way of REFWL.